Electronic Version

Stylesheet Version v1.1.1

INTEGRATED REDUNDANCY ARCHITECTURE AND METHOD FOR PROVIDING REDUNDANCY ALLOCATION TO AN EMBEDDED MEMORY SYSTEM

Abstract

An integrated redundancy architecture for an embedded memory system whereby a third memory element is added to the redundancy architecture such that all row and column fails may be stored in real-time. Architecture (20) includes a first memory element (22) (FME 22) having a register (24), a second memory element (26) (SME 26) having a register (28), a third memory element (30) (TME 30) having a register (32), and a finite state machine (34) (FSM 34) having a decision algorithm (36). FME (22), SME (26), TME (30), and FSM (34) are electrically connected to a built-in self-test (BIST) module (38). BIST module (38) outputs failed row and column addresses (40), also referred to as "fails," for rows and columns that are identified as defective during the BIST to the memory elements and FSM (34). FSM (34) allocates redundancy resources of the memory system according to decision algorithm

(36).